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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,352	02/26/2004	Yoko Sato	60538 (48229)	9123

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,352	SATO, YOKO	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,20,21 and 26* is/are pending in the application.

4a) Of the above claim(s) *21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,20 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/11/06 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 26 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is unclear where the originally filed specification provides support for "wherein the first semiconductor layer defines at least one trench that has a base part reaching the insulating layer and sidewalls extending through the insulating layer" as recited in the claim. In applicant's originally filed disclosure, neither the first semiconductor layer or the trench has sidewalls extending through the

insulating layer. See figures 1, 3 and 4. The insulating layer 10b (corresponding to the insulating layer of the claims) is continuous and does not have any other layers or their sidewalls extending therethrough.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 7, 8 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by JP-2001-351995 (cited by applicant).

With regard to claim 1, JP-2001-351995 discloses in figures 36 and 37, for example, a semiconductor device comprising:

- a support substrate 2;
- an insulating layer 3 formed on the support substrate;
- a first semiconductor layer 4 (left third of figure 36 and portion 42a of figure 37) formed on the insulating layer;
- a first high breakdown voltage transistor formed in the first semiconductor layer (either of the two transistors shown in the left third of figure 36 in high voltage region 42a);
- a second semiconductor layer 4 (left third of figure 36 and portion 42b of figure 37) formed on the insulating layer;

- a second high breakdown voltage transistor formed in the second semiconductor layer (either of the two transistors shown in the left third of figure 36 in high voltage region 42b);
- a first isolation region 45/47 formed between the first semiconductor layer and the second semiconductor layer, the first isolation region surrounding the first and second high breakdown voltage transistors individually and having a depth that reaches the insulating layer (as seen in figure 37, the isolation region 45/47 completely surrounds the different transistor regions 42a and 42b and is formed between the first and second semiconductor layers to the claimed depth);
- a third semiconductor layer 4 (middle third of figure 36 and any one of portions 44a-44f in figure 37) formed on the insulating layer;
- a first low breakdown voltage transistor formed in the third semiconductor layer;
- a second low breakdown voltage transistor formed in the third semiconductor layer; and
- a second isolation region 5 formed in the third semiconductor layer between the first low breakdown voltage transistor and the second low breakdown voltage transistor, the second isolation region having a depth that does not reach the insulating layer.

With regard to claim 2, JP-2001-351995 further discloses a third isolation region 45/47 formed between the second semiconductor layer and the third semiconductor layer, the third isolation region having a depth that reaches the insulating layer.

With regard to claims 3 and 4, the first, second and third semiconductor layer are all of equal thickness.

With regard to claims 7 and 8, the surfaces of the first, second and third semiconductor layers are at a same level.

With regard to claim 20, this claim is merely broader in scope than claim 1 and thus JP-2001-351995 discloses all the limitations therein. Note that the first isolation region 45/47 isolates the high breakdown voltage transistor (any transistor in region 42a of figure 37) from other transistors (any transistor in regions 42b, 42c, 42d, 43, 44a, 44b, 44c, 44d, 44e and 44f).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP-2001-351995, with evidence provided by Ning et al. (US 2004/0079993 A1).

JP-2001-351995 teaches the first, second and third semiconductor layers having the same thickness but is silent as to the thickness being 500 to 2000 nm. However, Official Notice is taken that it was well known to the skilled artisan at the time of the invention to form the semiconductor layers (SOI layers) to the claimed thickness. It is known to form the semiconductor layers to an large enough thickness to allow for

proper device operation while keeping the layer thin to save on material and processing costs. These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious). As evidence that it is well known to form SOI semiconductor layers to the claimed thickness, see Ning et al. paragraph [0019] which teaches that typical thicknesses for the top silicon layer in an SOI are from about 5 to about 2000 nm. Thus, Ning et al. provides evidence in support of the Examiner's statement of Official Notice.

8. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP-2001-351995 as applied to claims 1-4, 7, 8, 20 and 21 above, and further in view of Kojima (US 5,965,921).

JP-2001-351995 teaches the first and second high breakdown voltage transistors comprising a first gate insulating layer 6 formed above a channel region, but does not teach a second gate insulating layer formed above an offset region and thicker than the first gate insulating layer.

Kojima teach high voltage MOSFET's in figure 1. Kojima teach a first gate insulating layer 3E formed above a channel region and a second gate insulating layer (unlabeled, thick insulator above 3C) above an offset region 3C wherein the second gate insulating layer is thicker than the first gate insulating layer.

JP-2001-351995 and Kojima are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to one of ordinary skill in the art to form the first and second high breakdown voltage transistors of JP-2001-351995 with the first and second gate insulating layers as taught by Kojima. The motivation for doing so is to improve the short channel effect or to reduce the gate drain capacitance and gate-drain breakdown. Therefore, it would have been obvious to combine JP-2001-351995 with Kojima to obtain the invention of claims 9 and 10.

Response to Arguments

9. Applicant's arguments filed 8/11/06 have been fully considered but they are not persuasive.

Applicant argues that Shigenobu et al. does not disclose or suggest the first isolation region surrounding the first and second high breakdown voltage transistors *individually*. This is not persuasive. First, applicant states that in figure 36 the high-voltage transistors adjoin mutually. This is not an accurate reading of the reference since not all the high-voltage transistors are mutually adjoined. As clearly shown in figure 37 the high-voltage transistors are partitioned into multiple, mutually isolated sections 42a-42d. Each section might contain more than a single transistor, but the

transistors in the each section are isolated from the transistors in other sections. As explained in the rejection, the first and second high-voltage transistors are formed in separate semiconductor layers in separate sections (for instance the first high-voltage transistor is in section 42a and the second high-voltage transistor is formed in section 42b). Sections 42a and 42b are clearly isolated from each other by isolation region 45/47. As such, the first and second high-voltage transistors of the claims are surrounded by the first isolation region individually. Thus the rejection is considered proper.

Applicant also argues with regard to claim 20 that "Shigenobu et al. only shows memory cells having transistors with wells 47 without an oxide film as noted above." This argument is not well understood. First, an oxide film has not been noted above in applicant's response. Second, an oxide film is nowhere recited in claim 20. As such, it is unclear how this argument pertains to claim 20 or to the rejection thereof.

Applicant also argues that Shigenobu et al. does not disclose or suggest the first isolation region isolates the high breakdown voltage transistor from other transistors but instead shows multiple transistors surrounded by the isolation layer. This is not persuasive. First, any transistor formed in section 42a is isolated from other transistors in sections 42b, 42c, 42d, 43, 44a, 44b, 44c, 44d, 44e and 44f and thus the high breakdown voltage transistor in section 42a is indeed isolated from other transistors as recited in the claim. Second, claim 20 does not require the first transistor be isolated by the first isolation film from every other transistor formed but merely from some other transistors. As such, the rejection is considered proper.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N. DREW RICHARDS
PRIMARY EXAMINER